

CLAIMS

We claim:

- 1 1. An apparatus comprising:
2 a package, said package comprising a plurality of shelves;
3 a first semiconductor die electrically coupled to at least one of said shelves; and,
4 a second semiconductor die electrically coupled to at least one of said shelves,
5 wherein said second semiconductor die is above said first semiconductor die.
- 1 2. The apparatus of claim 1 wherein said package comprises a ceramic pin grid
2 array (PGA) package.
- 1 3. The apparatus of claim 1 wherein said package comprises a plastic pin grid array
2 (PPGA) package.
- 1 4. The apparatus of claim 1 wherein said first semiconductor die is a central
2 processing unit (CPU) die.
- 1 5. The apparatus of claim 4 wherein said second semiconductor die is a memory
2 cache.
- 1 6. The apparatus of claim 1 wherein said package has a single chip footprint.

1 7. The apparatus of claim 1 wherein said first semiconductor die is wire bonded to
2 said at least one shelf.

1 8. The apparatus of claim 7 wherein said second semiconductor die is wire bonded
2 to said at least one shelf.

1 9. The apparatus of claim 1 wherein said second semiconductor die is electrically
2 attached to a substrate and said substrate is wire bonded to said at least one shelf.

1 10. The apparatus of claim 9 wherein said second semiconductor die is wire bonded
2 to said substrate.

1 11. The apparatus of claim 9 wherein said second semiconductor die is electrically
2 attached to said substrate by solder bumps.

1 12. The apparatus of claim 1 further comprising an encapsulant filling said package
2 above said second semiconductor die.

1 13. The apparatus of claim 12 wherein said second semiconductor die is attached to
2 said at least one shelf such that an open cavity protects said first semiconductor die.

1 14. An apparatus comprising:

2 a plurality of shelves, said package for housing a plurality of semiconductor dies
3 in a vertically stacked position such that said package has a single chip package
4 footprint;

5 a first semiconductor die electrically coupled to at least one of said shelves; and,
6 a second semiconductor die electrically coupled to at least one of said shelves,
7 wherein said second semiconductor die is as above said first semiconductor die.

1 15. The apparatus of claim 14 wherein said package comprises a ceramic pin grid
2 array (PGA) package.

1 16. The apparatus of claim 14 wherein said package comprises a plastic pin grid
2 array (PPGA) package.

1 17. The apparatus of claim 14 wherein said first semiconductor die is a central
2 processing unit (CPU) die.

1 18. The apparatus of claim 17 wherein said second semiconductor die is a memory
2 cache.

1 19. The apparatus of claim 14 further comprising an encapsulant filling said package
2 above said second semiconductor die.

1 20. The apparatus of claim 19 wherein said second semiconductor die is attached to
2 said at least one shelf such that an open cavity protects said first semiconductor die.

1 21. A method constructing a multi-chip package, comprising:

2 placing a first chip package on a first shelf;

3 electrically attaching said first chip package to said first shelf;

4 placing a second chip package on a second shelf wherein said second shelf is
5 stacked above said first shelf; and,

6 electrically attaching said second chip package to said second shelf.

1 22. The method of claim 21 further comprising the step of filling said package above
2 said second chip package with an encapsulant.

1 23. The method of claim 22 wherein said step of placing a second chip package on a
2 second shelf further comprises placing a second chip package on a second shelf with a
3 sealer such that a sealed open cavity below said second shelf protects said first chip
4 package.

1 24. The method of claim 21 wherein said step of placing a first chip package further
2 comprises placing CPU chip package on a first shelf.

1 25. The method of claim 21 wherein said step of placing a second chip package
2 further comprises placing a memory cache on a second shelf.

1 26. The method of claim 21 wherein said step of electrically attaching said first chip
2 package further comprises wire bonding said first chip package to said first shelf.

1 27. The method of claim 21 wherein said step of electrically attaching said second
2 chip package further comprises wire bonding said second chip package to said second
3 shelf.

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